REMARKS

Claims 1-20 are pending.

Claims 1-20 are rejected.

Claims 2, 3-4, 6-7, 9-10, 12, 13-14, 16-17, and 19-20 are amended to correct informalities.

The Applicants respectfully assert that the amendments to Claims 2, 3-4, 6-7, 9-10, 12, 13-14, 16-17, and 19-20 and incorporated by reference in any claims depending therefrom, are not narrowing amendments made for a reason related to the statutory requirements for a patent that will give rise to prosecution history estoppel. *See Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 122 S. Ct. 1831, 1839-40, 62 U.S.P.Q.2d 1705, 1711-12 (2002); 234 F.3d 555, 566, 56 U.S.P.Q.2d 1865, 1870 (Fed. Cir. 2001).

EXAMINER INTERVIEW

Applicant called the Examiner on November 22, 2005 to discuss the fact that her cited prior art U.S. Patent 6,711,719 to *Cohn et al.* (hereafter "*Cohn 1*") only has column numbers through 14, where she cites column numbers higher than 14 in her Office Action. The Examiner said she would review her Office Action and call back later in the day.

The Examiner called back on November 22, 2005 and indicated that citing *Cohn 1* was a mistake and should have been US Patent 6,687,883 to *Cohn et al.* (hereafter "*Cohn*"). The Examiner said we both will note this fact in our interview summaries for the record.

Applicant called the Examiner on December 28, 2005 to set up an interview date but failed to reach the Examiner.

The Applicant had an interview with the Examiner and her supervisor on January 6, 2006 to discuss the important issues that the Applicant needed to be emphasized. The Applicant suggested that Cohn was directed to controlling leakage by determining probabilities of logic input states and forcing logic states in selected circuitry to reduce leakage in circuitry. The Applicant pointed out that Claim 1 of the present invention was directed to analyzing sensitivities of leakage power to IC parameters including process, circuit, and environmental and modifying selected of these parameters based on analysis of the sensitivities to reduce leakage power. Other features of the invention including using any leakage power margin to improve performance of timing critical circuitry and how the present invention determines leakage power sensitivity was also discussed.

The Examiner's supervisor said they would take the Applicant's comments into consideration when reviewing the written response. The Applicant thanked the Examiner and her supervisor for their time and helpful comments.

Applicant called the Examiner on January 3, 2006 to follow up on the message requesting an interview. The Examiner stated that I needed to send an official Fax with an agenda to schedule an interview. We scheduled the interview for January 6, 2006 at 10:00.

I. REJECTION UNDER 35 U.S.C. § 102

The Examiner rejected Claims 1-20 under *35 U.S.C. § 102(e)* as being anticipated by *Cohn*.

For a reference to anticipate a claimed invention, the reference must disclose every aspect of the claimed invention. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989).

Claim 1 is directed to a method of designing an IC having IC parameters including process, circuit, and environmental design parameters, wherein the method comprises 5 steps. For a patent to anticipate the invention of Claim 1 it must recite all of the claim steps. The Examiner states that *Cohn* anticipates Claim 1 and thus must show that all of the steps of Claim 1 are found in *Cohn*. The Examiner cites *Cohn*, column 1, lines 8-12 to support his assertion that *Cohn* is directed to an IC with IC parameters comprising process, circuit, and environmental design parameters. *Cohn*, column 1, lines 8-12 describes the field of his invention and does not mention process, circuit, and environmental design parameters but rather states; "this invention relates generally to semiconductor devices, and more specifically, to a system and method for reducing leakage current in a semiconductor device by providing reduction control circuitry in accordance with a probability determination." In particular, *Cohn* recites in his Summary of the Invention that his invention is directed to reducing leakage by forcing logic states based on probabilistic analysis of input states. Nowhere does *Cohn* teach or suggest the step of using leakage power sensitivity analysis of process, circuit, and environmental design parameters of an IC as recited in Claim 1 of the present invention.

Claim 1 of the present invention selects first parameters from the IC parameters in response to analyzing the average leakage power sensitivities and reduces a leakage power for one or more selected circuit macros of the IC by modifying one or more of the first parameters. *Cohn* reduces leakage by analyzing the probability of logic state

occurrences and then forcing states on logic gates based on this probabilistic analysis. While *Cohn* does teach a method of reducing leakage it is not a method that teaches the steps recited in Claim 1 of the present invention.

Therefore, the Applicant respectfully asserts that the rejection of Claim 1 under *35 U.S.C. § 102(e)* as being anticipated by *Cohn* is traversed by the above argument.

Claim 2 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 2 adds the limitation that the circuit macros, whose IC parameter sensitivities have been determined, are classified as timing non-critical circuit macros and timing critical circuit macros, wherein the timing non-critical circuit macros may have the IC parameters modified without significantly affecting an overall IC performance. The Examiner states that *Cohn* teaches Claim 2 and cites column 17, lines 50-53 and 57-58. In this recitation, *Cohn* states that timing critical gates have a size which is related to the size of its output net and to its timing requirements (e.g., more timing critical gates will be larger). While the size of the FET devices used to configure a logic gate normally relates to the logic gate's current drive capability and thus assures more current to drive large nets, it may not be the only criteria that determines if a circuit macro is timing critical. Regardless, *Cohn* does not teach or suggest classifying circuit macros, whose IC parameters have been determined, as circuit macros that may have these IC parameters adjusted without affecting an overall IC performance.

Therefore, the Applicant respectfully asserts that the rejection of Claim 2 under *35 U.S.C. § 102(e)* as being anticipated by *Cohn* is traversed by the above argument and for the same reasons as Claim 1.

Claim 3 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 3 adds the limitation that the one or more selected circuit macros of Claim 1 correspond to timing non-critical circuit macros. The Examiner states that *Cohn* teaches Claim 3 and cites column 2, lines 18-23. In this recitation, *Cohn* states; "it would therefore be highly desirable to provide improved methods and mechanisms for finding a low leakage vector by using probabilistic approaches to find the expected leakage of integrated circuit devices at any point in time, based on logic state statistics." Nowhere

does *Cohn* mention using the IC parameters of Claim 1 to reduce leakage, wherein timing non-critical circuit macros are selected to have their IC parameters modified based on a leakage sensitivity analysis of these parameters.

Therefore, the Applicant respectfully asserts that the rejection of Claim 3 under *35 U.S.C. § 102(e)* as being anticipated by *Cohn* is traversed by the above argument and for the same reasons as Claim 1.

Claim 4 has been amended to correctly depend from Claim 2. Claim 4 is indirectly dependent from Claim 1 and contains all the limitations of Claim 1. Claim 4 adds the step of determining a power dissipation margin as a difference between a first design power dissipation for the IC and a second power dissipation determined for the IC after the step of reducing said leakage power (by modifying one or more of the first parameters). The Examiner states that *Cohn* teaches Claim 4 and cites column 20, lines 59-67. This recitation is two steps Claim 21 of *Cohn*. In this recitation, *Cohn* states; "the method for reducing leakage power of a logic network as claimed in claim 20, wherein said forcing step further includes: forcing several nets to logic values simultaneously, said forcing step comprising the steps of: independently setting each net to both a logic zero (0) and logic one (1) and determining a change in expected power dissipation in each setting;". *Cohn* states that he determines a change in expected power dissipation after each of his forcing steps, wherein he forces logic states on selected gates after doing his probabilistic analysis. Claim 4 determines the change in power dissipation of the IC after the step of reducing a leakage power for one or more selected circuit macros of the circuit macros of said IC by modifying one or more of the first parameters as recited in Claim 1. While the present invention and *Cohn* both determine a change in power dissipation, the determination is done after two completely different methods of reducing leakage power.

Therefore, the Applicant respectfully asserts that the rejection of Claim 4 under *35 U.S.C. § 102(e)* as being anticipated by *Cohn* is traversed by the above argument and for the same reasons as Claim 1.

Claim 5 is dependent from Claim 4 and contains all the limitations of Claim 4. Claim 5 adds the step of redesigning one of the circuit macros corresponding to the timing-critical circuit macros using the power dissipation margin to improve a performance of the redesigned circuit macro while keeping the overall IC power substantially equal to or below the first design power dissipation for the IC. Claim 5 recites a step where the power dissipation saved by reducing the power of a timing non-critical circuit macro by modifying selected IC parameters is allocated to a timing-critical circuit macro whose performance is increased at a cost of additional power, wherein the total power of the IC is kept equal to or below a value before the leakage power was reduced. The Examiner states that *Cohn* teaches Claim 5 and cites column 18, lines 14-16 and lines 30-34. In the first recitation, *Cohn* describes adding an input to a high leakage gate to reduce the leakage of that gate not to improve its performance as recited in Claim 5. In the second recitation, *Cohn* is further describing adding an input to a macro with an (sic) observability don' t care (ODC) to reduce leakage and not to improve its performance as recited in Claim 5.

Therefore, the Applicant respectfully asserts that the rejection of Claim 5 under *35 U.S.C. § 102(e)* as being anticipated by *Cohn* is traversed by the above argument and for the same reasons as Claims 1 and 4.

Claim 6 has been amended to correct informalities. Claim 6 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 6 defines how the average leakage power sensitivity recited in Claim 1 is determined using 6 steps. The average leakage power sensitivity of Claim 1 defines the how leakage power varies when one or more of the IC parameters, including process, circuit, and environmental design parameters, are varied. The Examiner states that *Cohn* teaches the invention of Claim 6. The Applicant has shown that *Cohn* does not teach leakage power sensitivity to the IC parameters of Claim 1, rather, *Cohn* teaches a leakage power sensitivity to the various logic states at the input of logic gates or macros. While the present invention includes a step of determining occurrence probabilities for each input node of the circuit macros and a step of calculating state occurrence probabilities for each cell within the circuit macros,

this is in addition to the steps not taught by *Cohn*. The Applicant asserts that *Cohn* does not teach all of the steps of Claim 6 and therefore does not anticipate the invention of Claim 6.

Therefore, the Applicant respectfully asserts that the rejection of Claim 6 under *35 U.S.C. § 102(e)* as being anticipated by *Cohn* is traversed by the above argument and for the same reasons as Claim 1.

Claim 7 is dependent from Claim 6 and contains all the limitations of Claim 6 and Claim 1. Claim 7 adds the limitation that the leakage data and the leakage power sensitivity data for the IC parameters for the cell inputs are predetermined by using circuit analysis and circuit simulation tools. The Examiner states that *Cohn* teaches the invention of Claim 7 and cites *Cohn*, column 4, lines 21-24. The Applicant has shown that *Cohn* does not teach or suggest leakage power sensitivity data for the IC parameters of Claim 1. In the recitation of *Cohn*, column 4, lines 21-24, *Cohn* states that simulation is performed to force the nets to a particular value, and does not teach or suggest using simulation to determine leakage power sensitivity for the IC parameters as recited in Claim 1 of the present invention.

Therefore, the Applicant respectfully asserts that the rejection of Claim 7 under *35 U.S.C. § 102(e)* as being anticipated by *Cohn* is traversed by the above argument and for the same reasons as Claim 1.

Claim 8 is dependent from Claim 6 and contains all the limitations of Claim 6 and Claim 1. Claim 8 adds the steps for calculating the average leakage current of Claim 6. The Applicant has shown that *Cohn* does not teach the invention of Claim 6. The steps of Claim 8 are in addition to steps of Claim 6 not taught or suggested by *Cohn*. The Applicant, therefore, respectfully asserts that since *Cohn* does not teach all of the steps of Claim 8, *Cohn* does not anticipate the invention of Claim 8.

Therefore, the Applicant respectfully asserts that the rejection of Claim 8 under *35 U.S.C. § 102(e)* as being anticipated by *Cohn* is traversed by the above argument and for the same reasons as Claim 1.

Claim 9 is dependent from Claim 6 and contains all the limitations of Claim 6 and Claim 1. Claim 9 adds the steps for calculating the average leakage power sensitivity for a parameter P of said IC parameters of Claim 6. The Applicant has shown that *Cohn* does not teach the invention of Claim 6. The steps of Claim 9 are in addition to steps of Claim 6 not taught or suggested by *Cohn*. The Applicant, therefore, respectfully asserts that since *Cohn* does not teach all of the steps of Claim 9, *Cohn* does not anticipate the invention of Claim 9.

Therefore, the Applicant respectfully asserts that the rejection of Claim 9 under *35 U.S.C. § 102(e)* as being anticipated by *Cohn* is traversed by the above argument and for the same reasons as Claim 1.

Claim 10 is dependent from Claim 6 and contains all the limitations of Claim 6 and Claim 1. Claim 10 further adds the steps to the steps of Claim 6. The Applicant has shown that *Cohn* does not teach the invention of Claim 6. The steps of Claim 10 are in addition to steps of Claim 6 not taught or suggested by *Cohn*. The Applicant, therefore, respectfully asserts that since *Cohn* does not teach all of the steps of Claim 10, *Cohn* does not anticipate the invention of Claim 10.

Therefore, the Applicant respectfully asserts that the rejection of Claim 10 under *35 U.S.C. § 102(e)* as being anticipated by *Cohn* is traversed by the above argument and for the same reasons as Claim 1.

Claims 11-20 are directed to a computer program product implementing the steps of Claims 1-10. The Examiner rejected Claims 11-20 under *35 U.S.C. § 102(e)* as being anticipated by *Cohn* for the same reasons she rejected the corresponding method claim of Claims 1-10.

Therefore, the Applicant respectfully asserts that the rejections of Claims 11-20 under *35 U.S.C. § 102(e)* as being anticipated by *Cohn* are traversed for the same reasons as Claims 1-10.

II. CONCLUSION

The Applicant has traversed the rejections of Claims 1-20 under *35 U.S.C. 102(e)* as being anticipated by *Cohn*.

Claims 2, 3-4, 6-7, 9-10, 12, 13-14, 16-17, and 19-20 have been amended to correct informalities

The Applicant asserts that Claims 1-20 as amended are now in condition for allowance and request early allowance of these claims.

Applicants respectfully request that the Examiner call Applicant's attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining problems.

Respectfully submitted,

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